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09/444,819	11/22/1999	SHUICHI KIKUCHI	10417-006001	9133
26211	7590	07/28/2004	EXAMINER	
FISH & RICHARDSON P.C. 45 ROCKEFELLER PLAZA, SUITE 2800 NEW YORK, NY 10111			RAO, SHRINIVAS H	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/444,819

Applicant(s)

KIKUCHI ET AL.

Examiner

Steven H. Rao

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-4, 8-10, 17, 19 and 22-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-4, 8-10, 17, 19 and 22-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☒ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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***Priority***

Receipt is acknowledged of papers filed claiming priority from U.S. Serial No. 09/444819 filed on November 22, 1999 which itself claims priority from Japanese Patent Applications Heis 10-335877 filed on November 26, 1998, 10-345651 filed on December 04, 1998 and 10-351779 filed on December 12, 1998.

***Response to Amendment***

Applicants' amendment filed on February 13, 2004 has been entered on May 23, 2004, with the entry of the RCE.

Therefore claims 1,2,8 and 9 as amended by the amendment of February 13, 2004.

Claims 3-4,10,17,19 and 22-34 as previously recited are currently pending in the Application.

Claims 5-7,11-16,18 and 20-21 have been cancelled.

***Information Disclosure Statement***

Applicants' have not filed a IDS after the one filed on February 23, 2000.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

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said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

A. Claims 1-2,8 and 19 are rejected under 35 U.S.C. 103 as being obvious over Kwon et al. ( U.S. Patent No. 5,907,173 herein after Kwon) previously applied and further in view of Moslehi ( U.S. Patent No. 5,949,105 herein after Moslehi)

With respect to claim1 Kwon describes a semiconductor device including : a source region ( Kwon fig. 4 # 45, col. 5 line 41), a channel region ( Kwon fig.4 # area below gate 44), a drain region ( fig.4 # 47, col. 5 line 43), a gate electrode disposed above the channel region ( fig. 4 # 44, col. 5 line 44), and a drift region disposed adjacent to the channel region and extending to and below the drain region ( Fig.4 # 43), and wherein the first part of said drift region is formed shallowly at least below a substantial part of the gate electrode , and said first part has substantially uniform depth under said gate .

Kwon does not specifically describe the newly added limitation, “ wherein the entire first part of said drift region is located below the gate electrode “.

However, Moslehi in figure 1 etc. and col. 3 lines 47-53 describes the the entire first part of said drift region is located below the gate electrode to independently form the overlapped and the non-overlapped regions of the source and drain junctions which improves the device lifetime under hot-carrier stress and providing for better device performance and reliability characteristics .

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Moslehi's entire first part of said drift region is located below the gate electrode in Kwon's device to independently form the

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overlapped and the non-overlapped regions of the source and drain junctions which improves the device lifetime under hot-carrier stress and providing for better device performance and reliability characteristics . ( Moslehi col. 2 lines 14-60).

The remaining limitations of claim 1 are :

Wherein a second part of said drift region, having substantially uniform depth is formed more deeply than said first part and is located below the drain region. ( Kwon fig. 4 # 43, Moslehi figure1 #24 and 22 are below source/drain region 32/32 a).

With respect to claim 2, Kwon describes a semiconductor device including :

A first conductivity type well region formed in a first conductivity type semiconductor substrate ( Kwon fig. 1 p-well ), a gate electrode formed on the substrate via a gate insulating film (Fig.1 # 4-a gate electrode and # 32 gate insulating film), a first conductivity type body region ( fig. 1 # 6) formed adjacent to the gate electrode , a second conductivity type source region ( fig. 1 # 5) and a channel region formed in the first conductivity body region ( fig.1 region below gate 4), a second conductivity type drain region formed at a position remote from the first conductivity type body region. ( fig.1 # 7) and a two-part second conductivity type drift region, with the first part having substantially uniform depth, formed shallowly from the channel region to the drain region, at least below a substantial part of the gate electrode, ( Kwon fig.1).

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Kwon does not specifically describe the newly added limitation, " wherein the entire first part of said drift region is located below the gate electrode " .

However, Moslehi in figure 1 etc. and col. 3 lines 47-53 describes the the entire first part of said drift region is located below the gate electrode to independently form the overlapped and the non-overlapped regions of the source and drain junctions which improves the device lifetime under hot-carrier stress and providing for better device performance and reliability characteristics .

Therefore it would have been obvious to one of ordinary skill in the art at thte time of the invention to include Moslehi's entire first part of said drift region is located below the gate electrode in Kwon's device to independently form the overlapped and the non-overlapped regions of the source and drain junctions which improves the device lifetime under hot-carrier stress and providing for better device performance.

The remaining limitations of claim 2 are :

Wherein a second part of said drift region, having substantially uniform depth is formed more deeply than said first part and is below the drain region. ( Kwon fig. 4 # 43 and element 24 in Moslehi is below the drain region 32/32a. ).

With respect to claim 8, wherein a semiconductor device comprising a first Mos ( Kwon col. 1 line 19) transistor having a source region ( Kwon fig. 4 # 45, col. 5 line 41), a channel region ( Kwon fig.4 # area below gate 44), a drain region ( fig.4 # 47, col. 5 line 43), a gate electrode formed on the channel region ( fig. 4 # 44, col. 5 line 44), and a drift region formed between the channel region

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and the drain region ( Fig.4 # 43), and a second Mos transistor having a source region, a channel region, a drain region and a gate region formed on the channel region . (Kwon col.4 line 53 ) ; and wherein the drift region of the first Mos transistor is formed shallowly at least below the gate electrode but formed more deeply below the drain region. (Kwon fig. 4 ) ;

Kwon does not specifically describe the newly added limitation, " wherein the entire first part of said drift region is located below the gate electrode " .

However, Moslehi in figure 1 etc. and col. 3 lines 47-53 describes the the entire first part of said drift region is located below the gate electrode to independently form the overlapped and the non-overlapped regions of the source and drain junctions which improves the device lifetime under hot-carrier stress and providing for better device performance and reliability characteristics .

Therefore it would have been obvious to one of ordinary skill in the art at thte time of the invention to include Moslehi's entire first part of said drift region is located below the gate electrode in Kwon's device to independently form the overlapped and the non-overlapped regions of the source and drain junctions which improves the device lifetime under hot-carrier stress and providing for better device performance.

The remaining limitations of claim 8 are :

a source / drain region of the second MOS transistor consists of a low concentration source/drain region ( Kwon fig. 3 and col. 4 lines 63), a high concentration source-drain region ( Kwon col.5 line 4-5) and a middle concentration source/drain region whose concentration is higher than that of the

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low concentration source/drain region but lower than that of the high concentration source/drain region. (Kwon figs. 5 E to G).

With respect to claim 19, wherein the second conductive type drift region is formed to be adjacent to the first conductive type body region. ( Kwon figs. 1,4 etc.).

**B.** Claims 3-4, 9-10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,907,173 ( Kwon et al, herein after Kwon) and U.S. Patent No. 5,869,371 ( Blanchard et al., herein after Blanchard) as applied to claims 1-2,8 and 19 above, and further in view of U.S. Patent No. 5,949,106 ( Moslehi, herein after Moslehi).

With respect to claim 3, Kwon describes a semiconductor device including : second conductivity type drift region . ( Kwon figure 4 # 43, Moslehi fig. 1 # 24).

The limitation," wherein the second conductivity type drift region is formed by implanting at least two kind second conductivity type impurities which have different diffusion coefficients and at least one kind first conductivity type impurity which has a diffusion coefficient substantially equal to or larger than the diffusion coefficient of at least one kind second conductivity type impurity such that it is formed by diffusing the second conductivity type impurities in to a deep region by using a difference in the diffusion coefficients and is formed shallowly in a neighborhood of the source region by canceling the second conductivity type impurities by the first conductivity type impurity " in claim 3 is taken to be



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product-by –process limitations and non limiting. A product-by –process claim is directed to the product per se, no matter how actually made. See *In re Fessman* 180, USPQ 324, 326 ( CCPA 1974); *In re Marosi et al.* , 218 USPQ 289, 292 ( Fed. Cir. 1983) and *In re Thrope* 227 USPQ 964, 966 (Fed. Cir. 1985).

With respect to claim 4, wherein the second conductivity type drift region is formed by implanting an arsenic ion and a phosphorous ion as the second conductivity type impurities in to an overall surface region serving as the drift region ( Kwon fig. 5 d col. 6 lines 15-20) and selectively implanting a boron ion as the first conductivity type impurity only into a region in a neighborhood of the source region. ( Kwon fig. 5 d col. 6 lines 20-30).

The limitation," the second conductivity type drift region is formed by implanting an arsenic ion and a phosphorous ion as the second conductivity type impurities in to an overall surface region serving as the drift region and selectively implanting a boron ion as the first conductivity type impurity only into a region in a neighborhood of the source region. " in claim 4 is taken to be product-by –process limitations and non limiting. A product-by –process claim is directed to the product per se, no matter how actually made. See *In re Fessman* 180, USPQ 324, 326 ( CCPA 1974); *In re Marosi et al.* , 218 USPQ 289, 292 ( Fed. Cir. 1983) and *In re Thrope* 227 USPQ 964, 966 (Fed. Cir. 1985).

With respect to claim 9, wherein the a semiconductor device comprising a first Mos ( Kwon col. 1 line 19) transistor and a second Mos transistor (Kwon col.4 line 53 ) formed on the first conductivity type substrate (Kwon fig. 4) wherein the first Mos transistor includes a first conductivity type well region

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formed in the semiconductor substrate ( Kwon fig. 1 p-well ), a first gate electrode formed on the first conductivity type well region via a first gate insulating film (Fig.1 # 4-a gate electrode and # 32 gate insulating film), a first conductivity type body region ( fig. 1 # 6) formed adjacent to the gate electrode , a second conductivity type source region ( fig. 1 # 5) and a channel region formed in the first conductivity body region ( fig.1 region below gate 4), and a second conductivity type drain region ( Kwon fig. 1 # 7) region formed at a position remote from the first conductivity type body region (Kwon fig.1 # 7) a second conductivity type drift region formed shallowly from the channel region to the drain region, at least below the gate electrode and formed deeply below the drain region. ( Kwon fig.1).

Kwon does not specifically describe the newly added limitation, “ wherein the entire first part of said drift region is located below the gate electrode “.

However, Moslehi in figure 1 etc. and col. 3 lines 47-53 describes the the entire first part of said drift region is located below the gate electrode to independently form the overlapped and the non-overlapped regions of the source and drain junctions which improves the device lifetime under hot-carrier stress and providing for better device performance and reliability characteristics .

Therefore it would have been obvious to one of ordinary skill in the art at thte time of the invention to include Moslehi's entire first part of said drift region is located below the gate electrode in Kwon's device to independently form the overlapped and the non-overlapped regions of the source and drain junctions

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which improves the device lifetime under hot-carrier stress and providing for better device performance.

The remaining Limitations of claim 9 are :

Wherein the second Mos includes : a second conductivity type well region formed in the semiconductor substrate .

Kwon and Moslehi do not specifically mention a second conductivity type well.

However, Blanchard a patent from the same filed of endeavor, describes in fig.5 B etc. a second conductivity type well to provide deep body depths and spacing in relation to the epitaxial layer's depth and doping so that depletion boundaries from the body potential will pinch off the channel of the parasitic JFET and thereby protect the channel from high voltages.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Blanchard's second conductivity type well in Kwon's and Moslehi's device to provide deep body depths and spacing in relation to the epitaxial layer's depth and doping so that depletion boundaries from the body potential will pinch off the channel of the parasitic JFET and thereby protect the channel from high voltages. ( Blanchard col. 9 lines 40-50).

a second gate electrode formed on second conductivity type well region via a second gate insulating film (Blanchard fig. 2 F), and a source / drain region consisting of a low concentration source/drain region formed adjacent to the second gate electrode ( Kwon fig. 3 and col. 4 lines 63), a high concentration source-drain region ( Kwon col.5 line 4-5) and a middle concentration

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source/drain region whose concentration is higher than that of the low concentration source/drain region but lower than that of the high concentration source/drain region. (Kwon figs. 5 E to G).

With respect to claim 10, wherein the first Mos transistor consists of an N-Channel LDMOS transistor and the second Mos transistor consists of a P-Channel high breakdown voltage Mos transistor ( Kwon col. 4 lines 58- col. 5 lines 45).

With respect to claim 17, wherein the semiconductor device is arranged in plural via a element isolation film and a channel stopper layer is formed under the element isolation film. (Blanchard fig. 2g # 134, col. 6 line 14 and fig., 2G # 130, col. 6 line 14-15).

With respect to claims 20, 21 Kwon describes a semiconductor device in accordance with claim 1, wherein the entire first part of said drift region is located below said gate electrode. ( see rejection of claims 1,2,etc. above).

With respect to claims 22, 23 , Kwon describes a semiconductor device in accordance with claim 1, wherein the dopant concentration of said first part is higher than that of said second part. (Balnchard col. 4 line 54).

With respect to claim 24, a semiconductor device in accordance with claim 4, wherein the arsenic is implanted in the semiconductor substrate by an accelerating voltage of about 160 KeV at a dose of  $3 \times 10^{12}$  raised to  $12 \text{ cm}^2$ . ( Blanchard col. 4 lines 15-17, Kwon col. 5 lines 55-57).

With respect to claim 25, a semiconductor device in accordance with claim 8, wherein the low concentration source /drain region is formed by

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implanting boron in the semiconductor substrate at an accelerating voltage of about 160 KeV at a dose of  $3 \times 10^{15}$  raised to  $12 \text{ cm}^2$ . ( Blanchard col. 4 lines 15-17, Kwon col. 5 lines 55-57).

With respect to claim 26 a semiconductor device in accordance with claim 8, wherein the middle concentration source/drain region is formed by implanting boron in the semiconductor substrate at an accelerating voltage of about 40 KeV at a dose of  $5 \times 10^{15}$  raised to  $13 \text{ cm}^2$ . ( Blanchard col. 4 lines 15-17, Kwon col. 5 lines 55-57).

With respect to claim 27 a semiconductor device in accordance with claim 2, wherein the gate electrode has a thickness of about 2500 Å. ( Blanchard col. 4 lines 50-55).

With respect to claim 28 a semiconductor device in accordance with claim 1, wherein the source region is formed by implanting phosphorous in the semiconductor substrate at an accelerating voltage of about 40 KeV at a dose of  $3 \times 10^{15}$  raised to  $13 \text{ cm}^2$ . ( Blanchard col. 4 lines 15-17, Kwon col. 5 lines 55-57).

With respect to claim 29 a semiconductor device in accordance with claim 1, wherein the source region is formed by implanting phosphorous in the diffusion region at an accelerating voltage of about 40 KeV at a dose of  $3.5 \times 10^{15}$  raised to  $13 \text{ cm}^2$  and by implanting, arsenic at an accelerating voltage of about 80 KeV at a dose of  $5 \times 10^{15}$  raised to  $15 \text{ cm}^2$ , and the drain region is formed by implanting

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arsenic at an accelerating voltage of about 80KeV at a dose of  $5 \times 10^{15}$  raised to  $1.5 \times 10^{16}$  cm.<sup>-2</sup> ( Blanchard col. 4 lines 15-17, Kwon col. 5 lines 55-57).

With respect to claim 30 a semiconductor device in accordance with claim 1, wherein the drift region has an impurity concentration of about  $1 \times 10^{17}$  cm<sup>-3</sup>. ( Blanchard col. 7 lines 2-10).

With respect to claim 31 a semiconductor device in accordance with claim 17, wherein the size of the element isolation film is about 5um to 8 um and a distance from an end of the element isolation film to the channel stopper layer is about 2 um to 3 um. ( Blanchard col. 5 lines 20-25).

With respect to claim 32 a semiconductor device in accordance with claim 17, wherein the channel stopper layer is formed in the semiconductor substrate by implanting boron at an accelerating voltage of about 60 K.eV at a dose of  $5 \times 10^{15}$  raised to  $1.3 \times 10^{16}$  cm<sup>-2</sup>. ( Blanchard col. 4 lines 15-17, Kwon col. 5 lines 55-57).

### ***Response to Arguments***

Applicant's arguments filed 02/13/04 have been fully considered but they are not persuasive for the following reasons :

The outstanding rejection is based upon the combined teachings of Kwon and Moslehi wherein Kwon is the primary reference and Moslahi the secondary reference.

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The previous rejection cited Kwon figure 4 # 43 as the second part of said drift region having substantially uniform depth is formed more deeply than said first part and is located below the drain region.

Applicants' state, " the Office Action points to elements 26 and 24 in figure 1 of the Moslehi reference as corresponding to the two-part drift region recited in independent claims 1,2,8 and 9."

Applicants' argument that Moslehi's elements 26 and 24 in figure 1 is stated to be the two-part drift region is based on assumed rejection. The final rejection mailed 11/7/ 2003 (the last outstanding rejection , the advisory action of 5/7/04 is not relevant for the present issue) in pages 3-5 thereof merely mentions Moslehi's figure1 and other figures without identifying 26 and 24 as the two part drift region. Because by merely identifying elements 26 and 24, element 22 also a drift region is left out .

Further even element 24 in Moslehi is below the drain region 32/32a.

Moslehi col. 3 lines 47-55 ( describing figure 1) does indetify element 22 as the drain region, but rather regions 22, 24 and 26 are part of the drift region 20 with different doping concentration all of which are below the elevated drain region 32/32a.

Therefore both the applied references Kwon and Moslehi describe all the presently claimed elements and therefore are rejected.

Claims 2-4,9-10,17,19 and 22-34 were alleged to be allowable because of their dependency upon allowable independent claims.

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However as seen above the independent claims are not allowable therefore dependent claims 2-4,9-10,17,19 and 22-34 are also not allowable.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is ((571) 272-1718 . The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

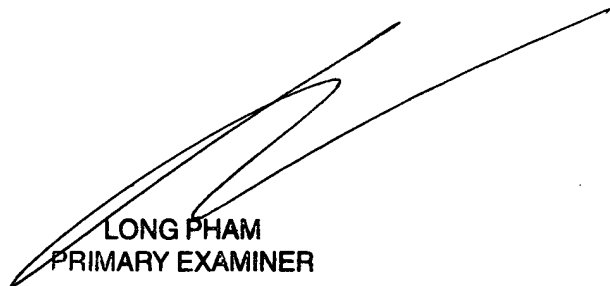


Steven H. Rao

Patent Examiner

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LONG PHAM  
PRIMARY EXAMINER